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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G11C 11/56 — A1

(11) International Publication Number: WO 95/20224

(43) International Publication Date: 27 July 1995 (27.07.95)

(21) International Application Number: PCT/GB95/00125

(22) International Filing Date: 23 January 1995 (23.01.95)

(30) Priority Data:
9401227.5 22 January 1994 (22.01.94) GB

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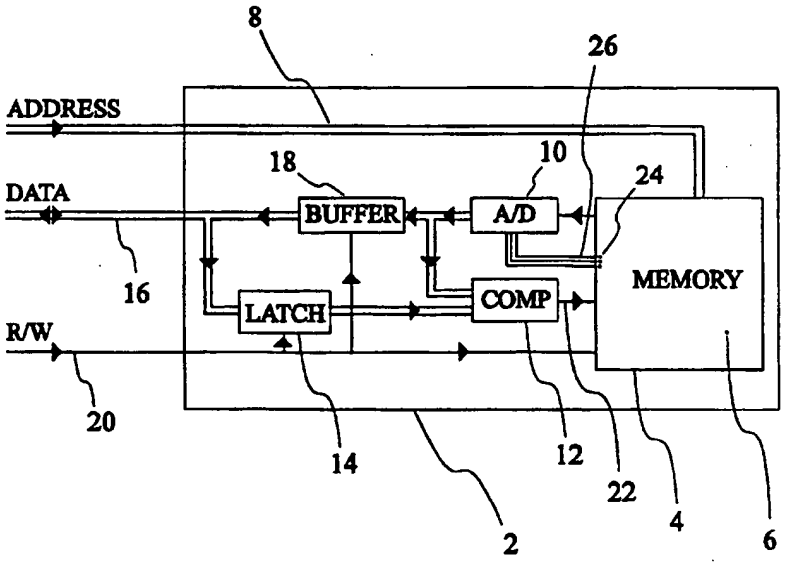
(81) Designated States: AM, AT, AU, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, EE, ES, FI, GB, GE, HU, JP, KE, KG, KP, KR, KZ, LK, LR, LT, LU, LV, MD, MG, MN, MW, MX, NL, NO, NZ, PL, PT, RO, RU, SD, SE, SI, SK, TJ, TT, UA, US, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG), ARIPO patent (KE, MW, SD, SZ).

Published
With international search report.

(54) Title: ANALOGUE MEMORY SYSTEM



(57) Abstract

A memory system (2) containing a main memory (4) with a large number of non-volatile memory cells (6), where each of the cells is capable of being charged or discharged in discrete amounts. There is also the means necessary for converting a digital signal, usually a sequence of bits (multiple data bits) sent by a host processor or other device, to an analogue signal for scaling the analogue signal according to reference cells, and for storing the analogue signal on one of the non-volatile memory cells. Recovery of the original digital signal (sequence of bits) is accomplished by reading the voltage value stored on the cell and converting it, using analogue to digital conversion techniques, to a digital signal corresponding to the original multiple data bits. This approach provides a reliable method of increasing the storage capacity of a solid state memory without the need for frequent refresh cycles.

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Analogue Memory System

The present invention relates to a non-volatile memory array system which can store information equivalent to two or more binary digits (bits) in each cell of the memory array. Designers are continually striving to increase the memory capacity of semiconductor memory arrays. The storage capacity of memory devices has increased substantially over the last few decades. Usually an increase in memory capacity is accompanied with an increase in the physical size of the memory; however, it would be better if the memory capacity could be increased with little or no increase in physical memory size.

Methods of increasing memory capacity have been developed in the past. One method which is commonly used to increase the memory storage capacity without changing the memory hardware is to use software data compression techniques. Typically, software data compression techniques are performed by the operating system of a computer. However, these data compression techniques can have a number of disadvantages, including slower read and write operations, and also the need to retain a portion of the data in uncompressed form. One of the reasons for slower read and write operations with some compression techniques is that the compression operation occurs prior to the storage operation, i.e. the two form a serial process.

Another method of increasing the memory capacity is to use multi-level storage. This technique is used to store two or more bits onto one analogue cell. US patent numbers 4,989,179 and 4,890,259 disclose the use of EEPROMs as analogue memories for storing analogue signals. The invention is directed towards analogue signal recording and playback, i.e. the signal is never converted to the digital domain. This method is used in applications where individual bit errors would not be disastrous, for example in recording voice messages on answering machines. However, this method could not be used successfully in applications

which rely on the integrity of each data bit stored because of the possibility of drift in voltage with time. For example, if a 32 bit number was being stored on 4 memory cells (8 bits on each cell) then each cell would have to distinguish between 256 levels. For a cell with a programming range of approximately 5V this would demand levels separated by approximately 20mV. A single bit error in the most significant bit could cause an enormous error. In computer and similar applications, absolute precision is essential. Thus the inventions disclosed in the above patents would not be suitable for storing multiple bits of information on one memory cell for computer applications without substantial modification.

PCT patent application WO93/04506 discloses a new class of semiconductor materials which have a high concentration of modulatable free charge carriers. The material characteristics are such that information can be stored in single or multiple bits per cell. This new material is claimed to have improved thermal stability of data stored therein. However, like the EEPROM multi-level storage devices, the new material also suffers from charge drift over a period of time. Patent application WO93/04506 emphasizes that "Any drift with time, regardless of how small, cannot be tolerated and will continue to be a focal point in the development of this new class of memory elements." One countermeasure disclosed in patent application WO93/04506 for guaranteeing the integrity of data stored on the cell uses a refresh cycle. The refresh cycle involves a feedback loop which calculates and delivers a refresh signal pulse of the required voltage and duration to the required memory element to bring it back to a preselected value.

It is an object of the present invention to avoid or minimise one or more of the above disadvantages. It is another object of the present invention to provide a memory system which can store multiple bits of data on and retrieve multiple bits of data from individual cells of a non-

volatile memory without loss of information.

The present invention provides a means for reliable storage and retrieval of multiple bits of data on a single memory cell. It does not do this by necessarily improving the intrinsic properties of the storage devices but by including additional circuitry to overcome the problem of charge drift with time.

According to a first aspect of the present invention there is provided apparatus for storing digital data and comprising at least one non-volatile semiconductor memory device having a multiplicity of electrically readable, writeable, and erasable multi-bit storage cells, at least one reference cell for storing a reference signal level, signal writing means formed and arranged for applying to selected ones of the storage cells, any one of several different voltage levels to store multi-bit data therein, and control means for monitoring drift of the voltage level stored in the reference cell and for accordingly scaling data read from and written to the storage cells.

As used herein the expression "signal level" may indicate charge or voltage level above or below a reference level which could be a fully discharged or fully charged level, or the value of any other electrical property e.g. resistance, of the storage cell material above or below a reference level which can be modified in a non-volatile predetermined manner by the application of charge or voltage to said material.

The necessary logic may be contained in the memory system to convert the multiple binary digits to be stored on each cell into an analogue voltage or other signal which is programmed or written into non-volatile memory. As used herein "non-volatile memory" is memory which retains data even when power is removed. The memory system also contains logic to recover the original multiple binary digits by converting the analogue voltage or other signal stored on a memory cell

to a digital signal.

A benefit of the present invention is the dramatic increase in effective memory storage capacity for digital information without increasing either the physical size of the memory or the number of cells in the memory.

In one embodiment of the invention, a memory store contains a number, usually a large number, of non-volatile memory data storage cells, where each of the cells is capable of being charged or discharged in discrete amounts. There is also provided digital to analogue conversion means for converting a digital signal, usually a sequence of bits (multiple data bits), sent by a host processor or other device, to an analogue signal and storing the analogue signal on one of the non-volatile data storage cells of the memory device. Recovering the original binary digital signal (sequence of bits) is accomplished by reading the voltage value stored on the storage cell and converting it, using analogue to digital conversion means, to a binary digital signal corresponding to the original multiple data bits.

Thus the present invention may provide a semiconductor memory system comprising at least one non-volatile semiconductor memory device having a plurality of memory cells; digital to analogue conversion means for converting binary digits from a host processor or other device to an analogue signal that can be stored on one of the cells; analogue to digital conversion means for converting the voltage stored on the memory cell to a digital signal; buffer means for transmitting information from the analogue to digital conversion means to the host processor.

In accordance with the present invention reference cells are used to scale the signal values which are to be read from or written to the storage cells. Reading circuitry is included to read the reference cell signal values from the non-volatile semiconductor memory to the analogue to digital

conversion means for setting the value of any scaling to be applied to the normal data reading and writing operations. This approach provides a reliable method of increasing the storage capacity of a solid state memory without the need for frequent refresh cycles to counteract drift of signal levels stored in the solid state memory.

The present invention may be used with multi-bit storage cell systems having various capacities. It will be appreciated though that the problem of drift is particularly significant with higher density memory devices wherein each storage cell is used to store at least 4 bits, preferably at least 6 bits, e.g. 8 bits or more (corresponding to 16, 64, and 256 different signal levels).

Conveniently separate digital to analogue and analogue to digital conversion means are used. If desired though there could simply be used one analogue to digital conversion means which is used as it stands when reading data back from the storage cells, and is used in combination with a comparator when writing data to the cells by repeatedly reading the signal value on a cell as a progressively increasing (or decreasing) voltage or charge is applied thereto and comparing the digital value thereof with the digital value of the data to be stored, using said comparator, and halting any further increase (or decrease) when the signal value or the storage cell matches that of the incoming data. It will furthermore be appreciated that the analogue to digital conversion means (ADC) may be implemented in various different ways including: a digital to analogue converter (DAC) in combination with a counter which progressively increments its count value, the digital output thereof being repeatedly converted to an analogue input until the counter count value and the analogue value to be converted match whereupon the counter is stopped.

It will be understood that the system of the present invention may contain more than one memory device or chip i.e. a bank of say 8 or 16 of these, which could all be

served by a common analogue to digital converter, buffer means, etc.

For a better understanding of the present invention and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings, in which:

Figure 1 shows a first memory system embodying the present invention; and

Figure 2 shows a second memory system embodying the present invention.

Figure 1 shows a memory system 2 having a main memory 4 containing an array of EEPROM data storage cells 6, though the same embodiment may be used with FLASH or UVEPROM technologies in any form factor, or it could be used with non-FET (Field Effect Transistor) technologies such as chalcogenide phase change materials. An address bus 8 connects the host processor and the main memory 4 and is used to address the EEPROM storage cells 6 in the main memory 4 in a known manner. An analogue to digital (A/D) converter 10, which could be a parallel encoder, is used when reading signal, voltage, levels from storage cells 6 and is also used to determine when a particular one of the EEPROM cells 6 in the main memory 4 is charged to a level corresponding to the multi-bit value to be stored in that cell. This is done with the aid of a comparator 12 by repeatedly reading the signal, voltage, level to which the storage cell has been charged, during application of a progressively increasing (or decreasing) voltage level thereto; comparing the multi-bit data value corresponding thereto as indicated by the analogue to digital converter 10; and halting any further increase (or decrease) in the applied voltage level when the multi-bit data value which has been read back corresponds to that which is to be stored. This obviates the need for a digital to analogue converter for converting the digital data to be stored into an analogue form before writing of the data into the storage cells 6. A data latch 14 is used during data writing to

hold data for the "reference" inputs to the comparator 12. A buffer unit 18 is provided between the output of the A/D converter 10 and a bi-directional data bus 16 connecting the memory system 2 to the host processor.

Within the memory system the data bus 16 connects to both the buffer 18 and the data latch 14. A read/write control line 20 from the host processor to the memory system is connected to the data latch 14, the buffer unit 18, and the main memory 4. A charge control line 22 connects the output of the comparator 12 to the main memory 4. One or more reference cells 24 are also contained within the main memory 4. The reference cells 24 are standard EEPROM cells. Each reference cell 24 is connected by a dedicated reference line 26, to the A/D converter 10.

The system is based on the fact that an EEPROM memory cell can be programmed with any one of a large number of different voltage levels on each cell rather than merely recording a binary logic level. The result is that the EEPROM memory cell can be used as an analogue storage device rather than a digital storage device. The EEPROM memory array 1 used is a particular type of EEPROM memory array which is capable of storing discrete amounts of charge and can be programmed by adding small amounts of charge in an iterative charging process.

EEPROM memory arrays are normally based on MOSFET devices. Programming these devices causes the conductivity of the MOSFET to vary and so the voltage measured at the drain end of the transistor (the output voltage) can be varied. To charge the cell to the correct voltage, small amounts of charge are added and the resulting new voltage level checked, this process being repeated until the required voltage is reached. A FLASH memory could be used instead of an EEPROM memory, in a generally similar manner except that a FLASH memory cell is charged fully initially and then discharged in small quantities until the correct voltage is reached. If FLASH memory was used then the present

invention would need only minor modifications. Similarly, the present invention could also be used with other non-volatile, discretely programmable memory devices such as chalcogenide phase charge materials as described in W093/04506 referred to hereinbefore.

Charge stored in an EEPROM cell will decay with time, but according to figures recently published charge decay is less then 2% over a period equivalent to 13 years at a temperature of 125°C. Nevertheless, whilst the effects of such drift may be acceptable for some applications, such as voice recording, countermeasures are essential for other applications, such as high density data storage.

In one embodiment of the present invention only one reference cell is included, and all read and write voltage values are scaled by this one reference cell. In yet another embodiment of this invention a plurality of reference cells are included. In order to provide the most appropriate scaling for each of the possible signal levels writable to the storage cells there may be used 2^n-1 reference cells where n is the number of binary digits which are to be stored on each multi-bit memory cell, with each reference cell containing a different one of the possible permutations of the binary digits (no reference cell is required for the zero voltage level).

One embodiment of this device will now be described by way of example, with reference to Figure 1 of the accompanying drawings.

The number of binary digits which are stored on a memory cell depends on the system configuration. In this example embodiment the equivalent of two bits of data are stored on each memory cell, although with minor modifications to the design a greater number of bits of information could be converted to an analogue signal and then stored at a particular location.

During a typical write cycle two bits of data are sent from the host processor onto the data bus 16, the appropriate address is put on the address bus 8, and the read/write control line 20 is set for write mode. When the read/write line is set for write mode then the buffer unit 18 is disabled and the data latch 14 is enabled. The data on the data bus 16 is then read into the latch unit 14. The EEPROM cell charging process is then initiated. The EEPROM memory location accessed by the address on the address bus 8 is then charged. As this occurs the A/D convertor 10 (which is a flash type A/D converter in this embodiment) repeatedly monitors the voltage actually stored on the memory cell and produces the digital equivalent at its output. The output of the A/D converter 10 is repeatedly compared with the contents of the data latch 14 by the comparator 12. When the output of the A/D 10 matches the contents of the data latch 14 then the charge control line 22 is set inactive and the charging process is stopped.

During a typical read cycle the host processor sets the read/write line 20 for read mode and puts the appropriate address of main memory 4 to be read onto the address bus 8. When the read/write line is set for read mode the buffer unit 18 is enabled and the data latch 14 is disabled. The analogue signal stored at the location accessed by the contents of the address bus 8 is then read and transferred via the A/D converter 10 to the buffer 18 as two binary digits. The buffer 18 then puts these two digital bits onto the data bus 16 and sends them to the host processor.

The reference cell 24 has a corresponding reference line 26 connected to the reference input of the A/D converter 10; this is shown diagrammatically in Figure 1. In practice it would not be necessary for any dedicated direct physical connection between a specific reference cell and the reference input of the A/D converter 10. There could simply be some logic provided to read the reference cell periodically and present the value to the reference input of the A/D converter 10. The reference cell may initially be

charged to the full value of the analogue signal voltage corresponding to the multi-bit data value to be "referenced", for example, for encoding two bits, the 11 level may correspond to 5V. After a period of time the charge stored may have drifted or decayed to 4.9V. If a cell is now to be charged to the 11 level then it must be charged to 4.9V to ensure that every cell on the array which stores the 11 level is charged to the same potential. By applying the reference cell value to the reference input of the A/D 10 all values are scaled according to the present charge level of the reference cell.

The use of just one reference cell would be acceptable in some applications, for example when only two or three bits are to be stored on each cell. However, the decay in charge is unlikely to be exactly linear. If just one reference cell is used as a scaling factor then all the values will be scaled linearly, whereas the rate of charge decay may be proportional to the amount of charge stored. This would limit the number of bits which could be stored on each cell. If higher densities of bit storage are desired then a number of reference cells are likely to be required.

In another embodiment of this invention, as shown in Figure 2, more than one reference cell is included. It should be emphasised that these reference cells are ordinary cells; they are not specially treated in any way, nor do they have any additional wiring or circuitry. Any cell in the array could be used as a reference cell, and the reference cells could be changed any number of times. The important point about a reference cell is that it is not available for storing data sent by the host processor. These reference cells are used to scale the values of voltage to be stored on an EEPROM cell, and also to scale the values of voltage read from an EEPROM cell.

In some applications 2n reference cells (where n is the number of different voltage levels than can represent data bits) might be used, perhaps more in others. If an EEPROM

array covered a large physical area then additional reference cells might be chosen according to physical location to help compensate for any areal variation in drift.

In the memory system of Figure 2 the address bus 8 goes into a reference applicator 28 which performs the necessary managerial functions for efficient operation of the memory system 2. A reference address bus 30 goes from the reference applicator 28 to the main memory 4. An internal data bus 32 connects the A/D converter 10, the comparator 12, a latch and write table unit 34, and a read-table and buffer unit 36. The read and write control line 20 goes to a control unit 38. A reference control line goes from the reference applicator 28 to the control unit 38. The output of the control unit 38 is an enable/disable line 42 which goes to the latch and write-table unit 34, the read-table and buffer unit 36, the comparator 12, and a read/write/charge control unit 44.

The reference applicator 28 performs various initialisation functions. The first of these initialisation functions is to write to certain reference cells. In this embodiment of the invention each voltage level which will be used to represent a series of data bits (including zero) will have its own reference cell. For two bit storage there will thus be four reference cells, one for each of the multi-bit values 00, 01 10 and 11 respectively. When the reference applicator charges the cell to the appropriate level it stores the two bit value and its corresponding voltage level in a look-up table within the read-table and buffer unit 36, and in a similar look-up table in the latch and write-table unit 34. The look-up table in the read-table and buffer unit 36 will have more entries than the latch and write-table unit 34 needs because the value to be written will correspond exactly to the value in the appropriate reference cell whereas the value read may be slightly different to the value at the corresponding reference cell because the decay in each cell will not be identical. After predetermined

time periods the reference applicator 28 reads the values of each reference cell and updates the appropriate entries for the look-up table in both the read-table and buffer unit 36 and the latch and write-table unit 34.

During a write operation, data from the host processor is input to the latch and write-table unit 34. The control unit 38 responds to the write request sent by the host processor by setting the enable/disable line 42 so that the latch and write-table unit 34 and the comparator are enabled and the read-table and buffer unit 36 is disabled. The data on the data bus 16 is used to access the look-up table within the latch and write-table unit 34, the entry corresponding to this data value (the voltage signal value to which the cell should be charged) is output to the reference input of the comparator 12. As with the embodiment of Figure 1 charging proceeds until the voltage system value stored on the cell equals the value on the reference input of the comparator.

During a read operation, the control unit 38 responds to the read request sent by the host processor by setting the enable/disable line 42 so that the latch and write-table unit 34 and the comparator are disabled and the read-table and buffer unit 36 is enabled. The appropriate memory cell is read and the digital output of the A/D converter 10 accesses the look-up table within the read-table and buffer unit 36 and the corresponding entry is output to the data bus 16 via a buffer within the read-table and buffer unit 36.

It will be appreciated that various modifications may be made to the above described embodiments within the scope of the present invention. Thus, for example, there may be used a chalcogenide material wherein the signal value is stored in the form of a resistance value by applying a corresponding charge or voltage. Also there would normally be used a significantly higher data storage density e.g. at least 8 bits per cell.

CLAIMS

1. Apparatus for storing digital data and comprising at least one non-volatile semiconductor memory device having a multiplicity of electrically readable and writeable multi-bit storage cells, at least one reference cell for storing a reference signal level, signal writing means formed and arranged for applying to selected ones of the storage cells any one of several different voltage levels to store multi-bit data therein, and control means for monitoring drift of the voltage level stored in the reference cell and for accordingly scaling data read from and written to the storage cells.

2. Apparatus according to claim 1, wherein the control means includes an analogue to digital converter for converting multi-bit form data read from the storage cells into binary digital form.

3. Apparatus according to claim 2, wherein the analogue to digital converter is a flash type (parallel encoding) converter.

4. Apparatus according to any one of the preceding claims, wherein the control means includes a comparator for comparing the analogue equivalent of received digital data with analogue data stored in the memory cells.

5. Apparatus according to claim 4 when dependent on claim 2 or claim 3 wherein said signal writing means is formed and arranged for applying voltage to said storage cells incrementally or decrementally and said control circuit means includes signal writing control means comprising a said comparator means formed and arranged for repeatedly comparing the signal level in a said storage cell, during incremental or decremental voltage level application thereto by reading the digital form thereof through said analogue to digital converter, with digital data to be stored in said storage cell, and halting incremental or decremental voltage level application to said storage cell when said signal level therein has reached a value corresponding to the multi-bit form of said digital data to be stored therein.

6. Apparatus according to any one of claims 2 to 5, wherein the analogue to digital converter comprises a counter having its output connected to a digital to analogue converter.

7. Apparatus according to any one of claims 1 to 3, wherein the control means includes a digital to analogue converter for converting received binary digital data into analogue from for writing to the storage cells in multi-bit form.

8. Apparatus according to claim 6 or claim 7, wherein the digital to analogue converter is a flash type (parallel encoding) converter.

9. Apparatus according to any one of the preceding claims and having a plurality of said reference cells for storing a respective plurality of different voltage levels.

10. Apparatus according to any one of the preceding claims and having a plurality of reference cells disposed at different areas of the memory device.

11. Apparatus according to any one of the preceding claims, wherein the memory device is an EEPROM.

12. Apparatus according to any one of the preceding claims, wherein the memory device is a FLASH memory.

13. Apparatus according to any one of claims 1 to 10, wherein the memory device is an UVEPROM.

14. Apparatus according to any one of the preceding claims and which is in the form of a single integrated circuit.

15. Apparatus according to any one of the preceding claims formed and arranged for storing multi-bit data having at least 6 bits, in each said storage cell.

16. A semiconductor memory system comprising at least one non-volatile semiconductor memory device having a plurality of memory cells, analogue to digital conversion means, and digital to analogue conversion means; arranged to enable each non-volatile memory cell to store a voltage which is equivalent to more than one data bit and to convert the voltage stored on the cell back to the original data bits when required, and wherein there are used reference sites to store voltages associated with each combination of

data to be stored, for scaling reading and writing operations.

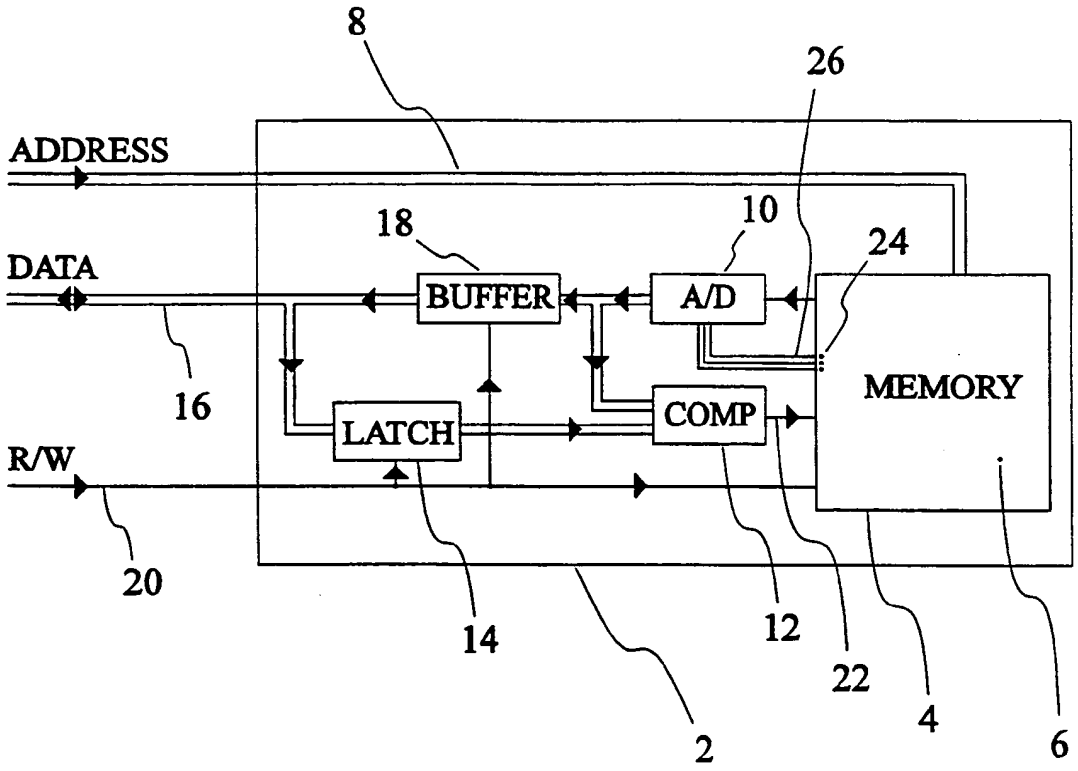

FIGURE 1

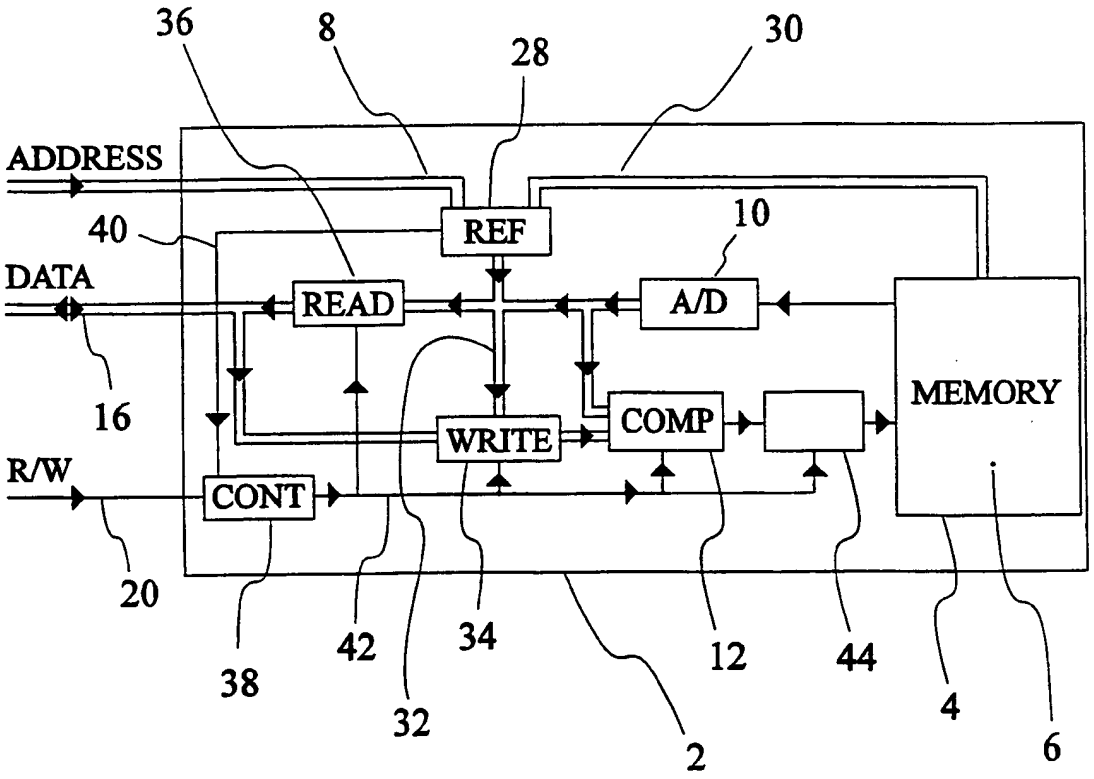

FIGURE 2

INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/GB 95/00125

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G11C11/56

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	WO,A,90 12400 (SUNDISK CORPORATION) 18 October 1990 see page 15, line 1 - page 42, line 2; figures 5-17; tables	1-3,9, 11,12,16 4-7,10, 13-15
X A	EP,A,0 349 775 (HARARI) 10 January 1990 see column 4, line 45 - column 9, line 7; figures 2A-E	1-3,11, 12 5,16
Y A	US,A,5 218 569 (BANKS) 8 June 1993 see column 7, line 15 - column 10, line 10; figures 5-8	4,5,13 1-3,11, 12,14,16
Y A	US,A,5 278 785 (HAZANI) 11 January 1994 see column 51, line 17 - column 56, line 45; figures 39-42	7,14,15 1,2,5,8, 11,16

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
6 April 1995	18.04.95

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INTERNATIONAL SEARCH REPORT

Int ional Application No
PCT/GB 95/00125

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	NOEL M. MORRIS 'Logic Circuits' 1983 , MCGRAW-HILL , LONDON,GB	6
A	see page 242, line 1 - page 249, line 9; figures 10.20,10.22-4	2-4
A	see page 239, line 24 - line 36; figure 10.18	7,8
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A	see page 312, left column, line 11 - page 314, left column, line 19; figures 3-7	1-3,9,16

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PCT/GB 95/00125

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